

# Notice of Allowability

Application No.

10/042,971

Examiner

Christopher E. Lee

Applicant(s)

JACOBSON, VAN

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Telephonic Interview conducted on 18<sup>th</sup> of January 2007.
2. ☒ The allowed claim(s) is/are 1-9, 11-19 and 32-46.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All b) ☐ Some\* c) ☐ None of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.


**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

## Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08),  
Paper No./Mail Date 11/29/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material

5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413),  
Paper No./Mail Date 20070118.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_.

  
Christopher E. Lee  
Primary Patent Examiner  
Art Unit 2111

### EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Brad Pedersen (Reg. No. 32,432) on 18<sup>th</sup> of January 2007.

The application has been amended as follows:

#### IN THE CLAIM

As to Claim 2, substitute "the response is stored in one of the first and second private memories in accessible by respective the second and the first CPUs" in lines 4-5 on page 3 in the Amendment filed on 27<sup>th</sup> of November 2006 by --the response is stored in one of the first and second private memories in accessible by the one of the first and second CPUs being coupled to the other one of the first and second private memories--.

#### ***Allowable Subject Matter***

2. The Examiner's statement of reasons for allowance had been discussed in the RCE Non-Final Office Action mailed on 25<sup>th</sup> of August 2006, such that:

With respect to claim 1, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that providing the communication stored in the shared memory directly to at least one of the first and second CPUs over the communication-interconnection mechanism without causing an interrupt of the operating system and' independently of the system I/O bus; executing at least one of the one or more processes on at least one of the first and second CPUs to generate at least a portion of the response to the communication; and receiving the generated portion of the response to the communication from

the at least one of the first and second CPUs in the respective private memories associated with each of the first and second CPUs.

The claims 2-9 are dependent claims of the claim 1.

With respect to claim 11, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that a first storage operatively connected to an incoming interface manager and a shared memory interface, the shared memory interface communicatively coupled to the plurality of CPUs via a communications interconnection mechanism, the incoming interface manager having an input coupled to the incoming communication interface output, the incoming interface manager operative for directly storing the communication received at the incoming interface manager input into the first storage independent of CPU intervention, the shared memory interface operative to provide shared access to the shared memory by the plurality of CPUs using the communications interconnection mechanism for retrieving at least a portion of the stored communication from the first storage and for providing the retrieved communication to at least one of the plurality of CPUs.

The claims 12-19 are dependent claims of the claim 11.

With respect to claim 32, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that an incoming shared memory operatively coupled to an input interface and a shared memory interface, the shared memory interface operatively coupled to the at least one main processing unit via a communications interconnection mechanism, the input interface operative to receive and store at least a portion of the communication in the incoming shared memory independently of the communications interconnection mechanism and independently of the operating system, the incoming shared memory operative to arbitrate shared access to the portion of the stored communication by the

at least one main processing unit independently of the input interface and unaccompanied by an interrupt to the operating system; and an outgoing shared memory operative to retrieve and selectively output the portion of the response from the private memory independently of the communications interconnection mechanism and unassisted by the operating system.

The claims 33-37 are dependent claims of the claim 32.

With respect to claim 38, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that a communications interconnection mechanism operably coupled to the one or more processing units and the shared memory via a shared memory interface, the communications interconnection mechanism operative to at least partially enable interprocessor communication and shared access to the shared memory by the one or more processing units wherein the input interface is adapted to perform the write operations and optionally update the software pointers, the one or more processing units configured to perform the read operations arbitrated by the shared memory interface such that each processing unit reads input communications stored in non-overlapping regions of the second portion of the physical storage locations for processing into a response written to the private memory via the process associated with the processing unit, the memory map characterized in that the first portion of the physical storage locations for write operations include physical storage locations devoid of input communications or storing input communications that have been read as a result of the read operations wherein the read and write operations avoid generating an interrupt to the first operating system environment and avoid inter-processor communication.

The claims 39-41 and 45 are dependent claims of the claim 38.

With respect to claim 42, Applicant's Admitted Prior Art (hereinafter AAPA) discloses a method for processing a communication in a computer system (i.e., computer system 150 of

Fig. 1B; See page 8, lines 9-12), wherein providing an input interface (e.g., I/O interface B of Fig. 1B) to a communications medium (i.e., Devices 178 of Fig. 1B); coupling a shared memory (i.e., Shared Memory 192 of Fig. 1B) to the input interface (in fact, said Shared Memory is coupled to said I/O interface B via said Front Side Bus in Fig. 1B), the shared memory (i.e., said Shared Memory) including one or more physical storage locations (See page 11, lines 4-7); operatively coupling a plurality of processors (i.e., CPU A 182, B 184, and C 186 in Fig. 1B) and a plurality of private memories (i.e., Private Memory A 198, B 194, and C 196 in Fig. 1B) to a communications interconnection mechanism (i.e., Front Side Bus 188 of Fig. 1B) and coupling the communications interconnection mechanism (i.e., said Front Side Bus) to the shared memory to enable the plurality of processors to share access to the shared memory (See page 10, lines 17-19) and enable each processor dedicated access to one of the plurality of private memories (See page 10, line 19); providing each processor with a process running under a first operating system (e.g., Solaris operating system; See page 9, line 17 through page 10, line 5). Slane [US 6,438,651 B1] discloses a method for managing requests to a cache (See col. 1, lines 7-10), wherein updating a set of software pointers (i.e., header 64 and tail 66 in Fig. 2) to at least a portion of physical storage locations so that a portion of a shared memory is organized as a circular buffer (i.e., circular data structure 62 of Fig. 2; See col. 3, lines 40-42); receiving an input communication and storing it directly into the circular buffer (i.e., enqueue operation) at a first tail location of the circular buffer (See col. 3, lines 53-55); and transferring the input communication (i.e., dequeue operation) at a head of the circular buffer (See col. 3, lines 55-57) to one of processing units (i.e., CPU in Queue User 52 of Fig. 3; See col. 3, lines 32-34). However, one of ordinary skill in the art would not have been motivated to modify the teachings of AAPA and Slane, alone or in combination with other references, in order to provide specific claimed method of executing the process to generate a response communication based upon

the input communication transferred to the processing unit; and storing the response in the private memory associated with the processing unit for transmission to the communication medium.

Therefore, the claim limitations are deemed allowable over the prior art as the prior art fails to teach or suggest that providing each processor with a process running under a first operating system; updating a set of software pointers to at least a portion of the physical storage locations so that a portion of the shared memory is organized as a circular buffer; receiving an input communication and storing it directly into the circular buffer at a first tail location of the circular buffer; transferring an input communication at a head of the circular buffer to one of the processing units; executing the process to generate a response communication based upon the input communication transferred to the processing unit; and storing the response in the private memory associated with the processing unit for transmission to the communication medium.

The claim 43 is a dependent claim of the claim 42.

With respect to claim 44, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that directly writing at least a portion of the incoming communication to the at least one writable location unassisted by the operating system; selectively allowing one of the plurality of processes to directly read at least the portion of the incoming communication from the at least one readable location avoiding interrupt generation to the operating system; and processing the retrieved portion of the incoming communication using the selected process to generate and store a response in the private memory avoiding inter-processor communication between the one or more CPUs.

The claim 46 is a dependent claim of the claim 44.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

**Conclusion**


3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on Monday through Friday, 9:00am - 5:00pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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